CLAIMS

What is claimed is:

Claim 1. A method of manufacturing a structure, comprising the steps of:

forming a first island of material having a first lattice constant;

forming a second island of material having a second lattice constant;

providing a mask over the first island and the second island which is used to form a tensile capping layer; and

forming at least a first finFET and a second finFET from the first island and the second island,

wherein the tensile capping layer prevents buckling one of the first and second finFET.

Claim 2. The method of claim 1, wherein the first island is comprised of SiGe material and the second island is comprised of Si:C material and the mask is a nitride hard mask.

Claim 3. The method of claim 1, wherein the first and second finFET are formed by sidewall image transfer and etching.

Claim 4. The method of claim 1, further comprising selectively growing an Si epitaxial sidewall layer on sidewalls of the first finFET and the second finFET, wherein the tensile

capping layer prevents buckling of the at least second finFET during the growth of the Si epitaxial sidewall layer thereon.

Claim 5. The method of claim 1, wherein:

etching forms the tensile capping layer from the hard mask on the first and second finFET;

the first finFET is comprised of SiGe and is placed in a tensile stress; and

the second finFET is comprised of is Si:C and is placed in a compressive stress.

Claim 6. The method of claim 5, wherein the tensile capping layer prevents collapse or buckling of the Si:C finFET.

Claim 7. The method of claim 1, further comprising:

forming shallow trench isolation (STI) in a substrate;

mixing the material into the substrate to form the first island and the second island by a thermal anneal process at a pFET region and a nFET region, respectively; and

wherein the STI relaxes and facilitates the relaxation of the first island and the second island.

Claim 8. The method of claim 1, wherein the first island is formed by one of depositing and growing Ge material and the second island is formed by one of depositing and growing Si:C or C material, the first island and the second island have a different relaxed crystal lattice.

Claim 9. The method of claim 4, wherein the Si epitaxial sidewall layer has a different lattice constant than the first material and the second material such that the selectively grown Si epitaxial sidewall layer will strain tensilely and compressively on the first island and the second island, respectively.

Claim 10. The method of claim 4, wherein the first finFET has a lattice constant $a \geq aSi$ and the second finFET has a lattice constant $a \leq aSi$.

Claim 11. The method of claim 1, wherein the first island is comprised substantially of SiGe and the second island is comprised substantially of Si:C and an epitaxially grown sidewall layer is grown on an etched SiGe finFET and Si:C finFET formed respectively from the SiGe island and the Si:C island, the SiGe finFET and the Si:C finFET is placed under a tensile stress and a compressive stress, respectively, by virtue of lattice matching of the epitaxially grown sidewall layer to the SiGe and Si:C finFET.

Claim 12. A method of manufacturing a semiconductor structure, comprising the steps of:

forming shallow trench isolation (STI) in a substrate with a first material;

forming a first island associated with a pFET region and a second island associated with an nFET region;

providing a hard mask in tensile stress over the pFET region and the nFET region;

forming a pFET fin and an nFET fin with a capping layer of the hard mask in the pFET region and the nFET region, respectively; and

growing sidewalls on the pFET fin and the nFET fin, wherein the capping layer prevents buckling of the nFET fin during sidewall growth.

Claim 13. The method of claim 12, wherein the pFET fin is made from a material comprised from SiGe and the nFET fin is made from a material comprised from one of Si:C or C.

Claim 14. The method of claim 13, wherein the SiGe becomes tensilely strained and the Si:C becomes compressively strained and the hard mask prevents buckling of the nFET fin by substantially countering the compressive stress form by sidewall formation thereon.

Claim 15. The method of claim 12, further comprising relaxing the STI and which facilitates relaxation of the first island and the second island during the thermally annealing step.

Claim 16. The method of claim 12, wherein the sidewalls are comprised of Si which has a different lattice constant than the pFET fin and the nFET fin such that the Si sidewall will tensilely and compressively stress the pFET fin and the nFET fin, respectively.

17. A structure, comprising:

a substrate;

a relaxed shallow trench isolation (STI) in the substrate;

a first finFET comprised of a first material having a first lattice constant and a cap of highly tensile material;

a second finFET comprised of a second material having a second lattice constant and a cap of highly tensile material; and

a Si epitaxially grown sidewall on the first finFET and the second finFET,

wherein the cap of highly tensile material on the second finFET prevents lateral buckling of the second finFET when the Si epitaxial sidewall is grown.

Claim 18. The structure of claim 17, wherein the first material is relaxed SiGe and the second material is relaxed Si:C.

Claim 19. The structure of claim 17, wherein the cap is comprised of nitride.

Claim 20. The structure of claim 17, wherein the STI is substantially relaxed and the first finFET is in tensile stress and the second finFET is in compressive stress.